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Time 3 Hours

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Maximum Marks 75

Note . Attempt all questions from Section A and two questions from Section B and two questions from Section C

Inst. The candidates are required to answer only in senal order. If there are many parts of a question, enswer them in continuation,

> SECTION - A (Short Answer Type Questions)

At questions are compulsory. Each question carries Note 3 marks

Simplify the Boolean function:

f = X'Y' + XY + X'Y

Explain full adder with truth table and logic circuit diagram.

Implement EX - OR Gate with NAND Gate only.

Express the Boolean function F = P + Q' R in a sum of minterns

Differentiate between Register and Latch.

Explain the working of ROM. Design 32 < 4 ROM structure.

Explain the working of JK Flip - Flop using logic diagram and excitation table.

How many 128 : 8 RAM chips are needed to provide a memory capacity of 2046 bytes?

A 4 bit binary up / down counter is in binary state of zero. Find the next state in down mode.

## SECTION - B (Long Answer Type Questions)

Note: Attempt any two questions. Each question carries 12 marks.

Let F(X, Y) = X' + Y. Simplify the expression for function:

F (F (A + B, B), C)

Simplify using K - map :  $F(A, B, C, D) = \Sigma(1, 3, 7, 11, 15)$  $d(A, B, C, D) = \Sigma(0, 2, 5)$ 

- What is a multiplexer and demultiplexer? Explain how an 8 x 1 multiplexer can designed using two 4 × 1 multiplexers
- What is decoder? Design a BCD to decimal decoder. 4.
  - Why NAND and NOR Gate is called Universal gate? Justify with
  - Convert RS Flip Flop to T-Flip Flop using excitation table

Note - Attempt any two questions. Each question carries 12 marks

implement the following function with a multiplexer  $F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$ 

- Design a counter that has repeated sequence of six States 0, 1, 2, 4. 6 and repeat using J – K flip flop.
- Write short notes on the following:
  - 4 Bit Register with Parallel load
  - (11) Implement Full Adder circuit with a decoder and two OR gates.
- Write short notes on any three of the following:
  - Block diagram of RAM and ROM
  - (ii) Cache memory
  - (iii) Virtual memory
  - Differentiate betrigen static RAM and dynamic RAM (iv)

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